REMARKS/ARGUMENTS

In this Amendment, Applicant amends claims 8 and 21 to better define the claimed invention by adding the recitation "wherein the method is implemented in a microprocessor." Applicant also amends claim 15 to correct typographical errors by amending the claim to recite "generates a whole increment value by outputting b bits of a first logic state for each b-bit group, b bits of the operand for each b-bit group, or b bits of an increment value for each b-bit group." Additionally, Applicant makes other amendments to the specification and claims 1-5, 7-21, and 23-28 to correct typographical errors, to correct translational errors, and/or to improve clarity. No new matter is introduced.

Prior to entry of this Amendment, claims 1-28 were pending in the application. After entry of this Amendment, claims 1-28 remain pending in the application.

In the Office Action, the Examiner rejected claims 8-14 and 21-26 under 35 U.S.C. § 101; rejected claims 15-20 under 35 U.S.C. § 112, ¶ 2; and allowed claims 1-7, 27, and 28. The Examiner also indicated that claims 15-20 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. § 112, ¶ 2.

Rejection Under 35 U.S.C. § 101

Applicant amends claims 8 and 21 to add the recitation "wherein the method is implemented in a microprocessor." At least partially as a result, Applicant submits that independent claims 8 and 21, as well as dependent claims 9-14 and 22-26, provide a practical application that produces a useful, tangible, and concrete result. As such, Applicant submits that this amendment overcomes the rejection of claims 8-14 and 21-26 under 35 U.S.C. § 101.

Rejection Under 35 U.S.C. § 112, ¶ 2

Applicant amends claim 15 to correct typographical errors by amending the claim to recite "generates a whole increment value by outputting b bits of a first logic state for each b-bit group, b bits of the operand for each b-bit group, or b bits of an increment value for each b-bit group." Applicant submits that this amendment overcomes the rejection of claims 15-20 under 35 U.S.C. § 112, ¶ 2.

Boolean Expressions 1 and 2

Applicant notes that a logic table associated with Boolean expressions 1 and 2 of an example embodiment appears below.

IN (decimal)	IN (binary)	IN_C (binary)	IN+1 (binary)	IN+1 (decimal)
0	0000	0101	0001	1
1	0001	0110	0010	2
2	0010	0111	0011	3
3	0011	0100	0100	4
4	0100	1001	0101	5
5	0101	1010	0110	6
6	0110	1011	0111	7
7	0111	1000	1000	8
8	1000	1101	1001	9
9	1001	1110	1010	10
10	1010	1111	1011	11
11	1011	1100	1100	12
12	1100	0001	1101	13
13	1101	0010	1110	14
14	1110	0011	1111	15
15	1111	0000	0000	0

In a first example, if the 4-bit group of the operand IN is 1011, then IN<3> = 1, IN<2> = 0, IN<1> = 1, and IN<0> = 1. As a result, IN_C<3> = IN<2> OR IN<3> = 1,

IN_C<2> = ~IN<2> = 1, IN_C<1> = IN<0> OR IN<1> = 0, and IN_C<0> = ~IN<0> = 0. Thus, IN_C = 1100.

Because IN<1> = 1 and IN<0> = 1, (IN+1)<3:2> = IN_C<3:2> and (IN+1)<1:0> = "00". Applicant notes that (IN+1)<3:2> = IN_C<3:2> means that, in this case, (IN+1)<3> = IN_C<3> = 1 and (IN+1)<2> = IN_C<2> = 1. And, as discussed above, (IN+1)<1> = 0 and (IN+1)<0> = 0. Therefore, in this case, the increment value IN+1 is 1100.

This example corresponds to part of Example 1 in paragraph [0027] of the specification. As can be seen in Example 1, the whole increment value is 1100, the 4 bits of the increment value IN+1 for this 4-bit group 1011 of the operand IN.

In a second example, if the 4-bit group of the operand IN is 0110, then IN<3> = 0, IN<2> = 1, IN<1> = 1, and IN<0> = 0. As a result, IN_C<3> = IN<2> OR IN<3> = 1, IN_C<2> = ~IN<2> = 0, IN_C<1> = IN<0> OR IN<1> = 1, and IN_C<0> = ~IN<0> = 1. Thus, IN_C = 1011.

Because IN<1> = 1 and IN<0> = 0, (IN+1)<3:2> = IN<3:2> and (IN+1)<1:0> = IN_C<1:0>. Applicant notes that (IN+1)<3:2> = IN<3:2> means that, in this case, (IN+1)<3> = IN<3> = 0 and (IN+1)<2> = IN<2> = 1. Similarly, (IN+1)<1> = IN_C<1> = 1 and (IN+1)<0> = IN_C<0> = 1. Therefore, in this case, the increment value IN+1 is 0111.

In a third example, if the 4-bit group of the operand IN is 1101, then IN<3> = 1, IN<2> = 1, IN<1> = 0, and IN<0> = 1. As a result, IN_C<3> = IN<2> OR IN<3> = 0, IN_C<2> = ~IN<2> = 0, IN_C<1> = IN<0> OR IN<1> = 1, and IN_C<0> = ~IN<0> = 0. Thus, IN_C = 0010.

Because IN<1> = 0 and IN<0> = 1, (IN+1)<3:2> = IN<3:2> and (IN+1)<1:0> = IN_C<1:0>. Applicant notes that (IN+1)<3:2> = IN<3:2> means that, in this case,

(IN+1)<3> = IN<3> = 1 and (IN+1)<2> = IN<2> = 1. Similarly, (IN+1)<1> = IN_C<1> = 1 and (IN+1)<0> = IN_C<0> = 0. Therefore, in this case, the increment value IN+1 is 1110.

These example illustrate sample calculations using Boolean expression 1, given by:

IF IN<0> and IN<1> = "1",

(IN+1)<3:2> = IN_C<3:2>,

(IN+1)<1:0> = "00",

IF IN<0> or IN<1> = "0",

(IN+1)<3:2> = IN<3:2>,

(IN+1)<1:0> = IN_C<1:0>;

and sample calculations using Boolean expression 2, given by:

IN_C<0> = ~IN<0>,

IN_C<1> = IN<0> OR IN<1>,

IN_C<2> = ~IN<2>,

IN_C<3> = IN<2> OR IN<3>.

Request for Reconsideration and Allowance

Accordingly, in view of the above amendments and remarks, reconsideration of the rejections and allowance of each of claims 1-28 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Director of the USPTO is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for

any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; in particular, extension of time fees.

Respectfully submitted,

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By _____

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